Microelectronic Engineering 199 (2018) 92–95

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Research paper

Self-aligned photolithography for the fabrication of flexible transparent high-voltage thin film transistors, diodes and inverters

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ARTICLE INFO

Keywords:
High-voltage device
Self-aligned photolithography
Flexible electronics
Transparent electronics

ABSTRACT

We report the realization of flexible fully-transparent high-voltage (HV) inverters composed with a high-voltage thin film transistor (HVTFT) drive and an on-chip high-voltage thin film diode (HVTFD) load. The overall fabrication temperatures are decreased as low as 75 °C to minimize the built-in strain caused by the large thermal expansion mismatch. High on/off ratio of 10^{10}, rectification ratio of 10^9 and voltage gain of 8.5 are achieved in the flexible HVTFT, HVTFD and HV inverter, respectively. In addition, the flexible HV devices are fabricated with a novel self-aligned photolithography technology, and the fabrication procedure and working principle are depicted in this letter. This work combines HV electronics with the upsurging flexible transparent electronics, and will initiate interdisciplinary researches between the two fields.

1. Introduction

High-voltage (HV) thin film transistors (TFTs) [1], thin film diodes (TFDs) [2] and inverters are indispensable building blocks in thin film circuits. Ubiquitous applications involve the driving circuits of piezoelectric actuators [3], integrated micro-electromechanical systems (MEMSs) [4, 5] and various display technologies, such as ferroelectric liquid crystals displays [6], electrophoretic displays [7], electro-optical displays [8] and field emission displays [9], as well as the readout circuits of X-ray imaging sensors [9]. Better yet, recent studies explored the emerging application of HVTFTs and HVTFDs in energy management circuits for building integrated photovoltaics (BIPVs) [11] and triboelectric nanogenerators (TENGs) [2]. Meanwhile, the incoming eras of internet of things and wearable electronics, where HV circuits have a great prospect of application [10], bring forward the demand of flexible and transparent electronics. In soft robotics [4], flexible displays [12] and sensors [13], HV circuits are expected to possess some degree of mechanical flexibility, while in photovoltaics [14], transparent or even fully-transparent circuits are favorable for higher conversion efficiency of solar cells. However, very few studies have been reported on flexible transparent HV circuits due to the lack of high-performance flexible device components. In fact, reports on oxide semiconductor HVTFTs [4, 11, 15–17] have been presented owing to their wide bandgaps and thus large breakdown field strengths [18]. Deficiently, high-temperature deposition or post-annealing treatment is required in these devices to improve the crystal quality, which is not feasible for the flexible transparent polymer substrates. Furthermore, so far there is no report on flexible transparent HVTFDs except our recent breakthrough [2]. Without on-chip HVTFT drive and HVTFD load, it is impossible to achieve integrated flexible transparent HV inverters and any other circuits.

This work reports flexible fully-transparent HV inverters composed with an HVTFT drive and an on-chip HVTFD load. High on/off ratio of 10^{10}, rectification ratio of 10^9 and voltage gain of 8.5 are achieved for HVTFTs, HVTFDs and HV inverters, respectively. In addition, the HV devices in this letter are fabricated with a novel self-aligned photolithography technology, which is proved to be effective in improving the uniformity and repeatability of HV devices. The fabrication procedure and working principle of the self-aligned photolithography are introduced, while the uniformity and repeatability data can be found elsewhere [19].

2. Experiments

The detailed fabrication procedure of the self-aligned photolithography process is illustrated in Fig. 1a-d. Step 1: a quartz carrier (500 μm thick) was prepared. Step 2: chromium (Cr, 50 nm thick) pattern was deposited onto the quartz carrier. Step 3:

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https://doi.org/10.1016/j.mee.2018.07.021
Received 1 June 2018; Received in revised form 10 July 2018; Accepted 30 July 2018
Available online 01 August 2018
0167-9317/ © 2018 Published by Elsevier B.V.

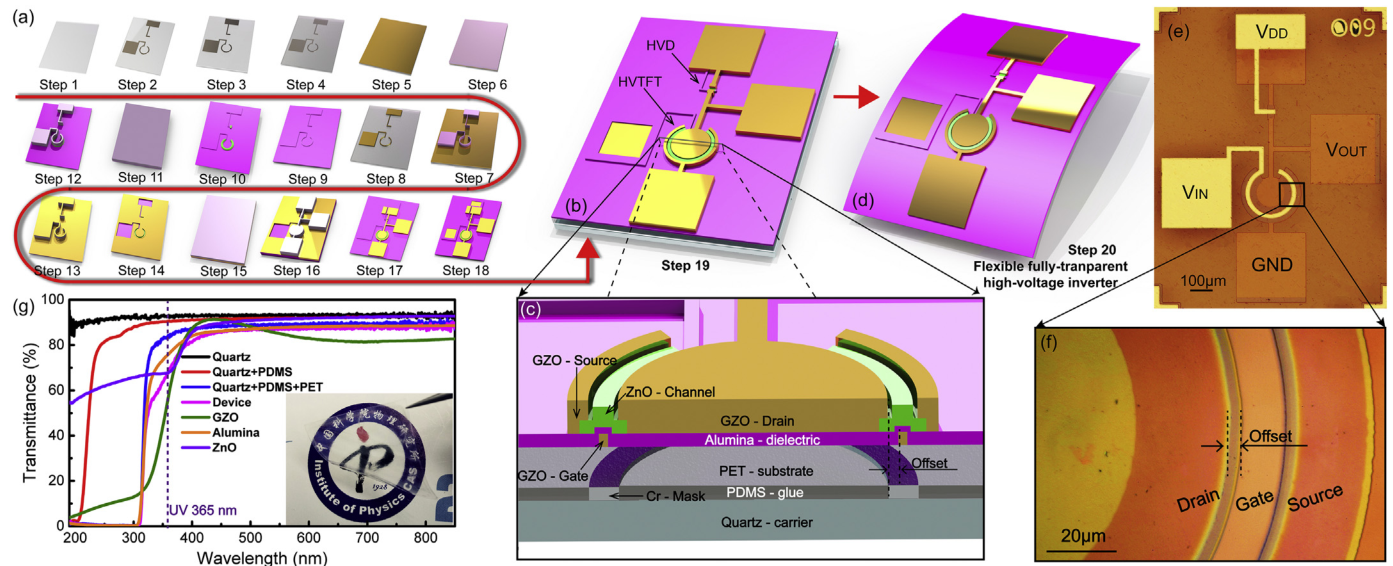

Fig. 1. (a) A typical fabrication procedure of self-aligned HV inverters. (b) Structure diagram of a self-aligned HV inverter before it was peeled off from the quartz carrier, which contains an HVTFT drive and an HVD load. (c) Cross-sectional view of an HVTFT. (d) Structure diagram of a flexible self-aligned HV inverter after it was peeled off from the quartz carrier. (e) Optical microscope image of a self-aligned HV inverter. (f) Local enlarged image of an HVTFT which shows the offset region between gate and drain. (g) Optical transmittance spectra of a completed 25 mm × 25 mm PET wafer and all the transparent materials involved in the fabrication. The inset is the photograph of the flexible fully-transparent devices.

polydimethylsiloxane (PDMS, mixture of the base and curing agent of Sylgard 184 in a proportion of 10:1) glue is spin-coated onto the quartz wafer. Step 4: polyethylene terephthalate (PET) substrate (50 μm thick) was stuck onto quartz carrier with the PDMS glue and cured at 75 °C for 3 h. Step 5: gallium zinc oxide (GZO, 100 nm thick) gate electrode layer was deposited onto the PET substrate. Step 6: AZ6130 positive photoresist was spin-coated onto GZO and baked at 75 °C. Step 7: the photoresist pattern was formed after backside exposure using the Cr pattern as mask (UV 365 nm, dose = 120 mJ/cm^2) and development. Step 8: etching of GZO using photoresist as mask and stripping of photoresist. Step 9: alumina (Al_2O_3, 100 nm thick) was deposited via atomic layer deposition (ALD) at 75 °C with trimethylaluminum (TMA) and water as precursors. Step 10: zinc oxide (ZnO, 40 nm thick) was deposited via radio frequency magnetron sputtering at room temperature in Ar/O_2 mixed atmosphere with a power of 70 W (2 in. target) and pressure of 0.4 Pa and patterned by photolithography and wet etching. Step 11: coating photoresist. Step 12: the photoresist pattern was formed after backside exposure with a smaller dose of 90 mJ/cm^2 and development. Step 13: GZO (100 nm thick) electrode layer was deposited onto the front side. Step 14: photoresist and the GZO on it were removed after lift-off. Step 15: coating photoresist. Step 16: patterning of the photoresist by photolithography. Step 17: wet etching of GZO and stripping of photoresist. Step 18: opening contact via holes. Step 19: shorting gate and drain of the HVTFD. Step 20: the flexible HV devices were completed after it was peeled off from the quartz carrier by dissolving the PDMS in dichloromethane (Fig. 1d). The maximum process temperature of the present self-aligned technology is 75 °C, which is fully compatible with current manufacturing process of flexible electronics.

The present HV inverter is constructed with an HVTFT drive and an HVTFD load (Fig. 1b). Unlike other reports which involve off-chip resistor load [4, 5, 20], an on-chip micro-scale HVTFD is employed for better scaling down and integration. The cross-sectional view (Fig. 1c) shows the structure diagram of the HVTFT, in which the channel length is almost the same as the Cr mask, whereas the gate length is shorter due to the overexposure in step 7. Fig. 1e shows an optical microscope picture of one completed HV inverter. A local enlarged picture of the HVTFT (Fig. 1f) shows that the offset length is approximately 3 μm. After peeling the flexible HV inverter off from the reusable quartz carrier, the device becomes flexible fully-transparent with a high transmittance over 80% in visible spectrum range (Fig. 1g).

The self-aligned photolithography, employed in this work, is a newly developed technology aimed for improving the uniformity and repeatability of HV devices. Distinguished from conventional self-aligned routes which utilize opaque gate on the front side of the transparent substrate as the mask in the backside exposure process [21, 22], opaque Cr mask is stuck onto the backside of the PET substrate with PDMS to facilitate the proximity exposure method [23], as shown in Fig. 2a. Fig. 2b shows the simulated exposure intensity inside the photoresist, where the shaded area is not necessarily in the same length as the Cr mask, but rather amendable through modulating the exposure dose. The exposure intensity contour of the Cr mask pattern is shown in Fig. 2c. In the proximity exposure method, there is a penumbral region, near the edge of the Cr mask, with the length $\delta = k(\lambda d)^{1/2}$ [24], where k is a process-related parameter, typically around 1, λ the wavelength of the exposure light and d the distance between mask and the photoresist, i.e., 365 nm and 50 μm in this work, respectively. A local enlarged contour and extracted intensity profiles are demonstrated in Fig. 2d, which are consistent with the experimental results from other report [25]. Obviously, intensity in the high dose case changes faster than that in the low dose case. Supposing a definite value for threshold dose (the minimum intensity of fully exposure), the width of the underexposed photoresist, which remains after development, will differ by 2 × offset length in the high and low dose cases (Fig. 2d). The presented self-aligned photolithography technology employs two times of backside exposure process, the first (step 7) for the gate etching and the second (step 12) for the source/drain lift-off. By modulating the exposure dose in the two exposure processes, offset region with desired length between the gate and drain can be achieved as expected.

Higher performances are realized with a lower fabrication temperature of 75 °C in this work, compared with 100 °C in our previous works [2, 26]. Fig. 3a shows the typical n-type transfer curves of the HVTFTs with high on/off ratios of 1.23 × 10^{10} and 1.67 × 10^{10} in the flat and bent test (V_{DS} = 10 V, radius = 12 mm), respectively. The turn on voltage (V_{ON}) and sub-threshold swing are 1.5 V and 0.43 V/dec in the flat test, while −1 V and 0.64 V/dec in the bent test. In the bending state, V_{ON} negatively shifts by 2.5 V and on current (I_{ON}) increases by two times compared to those in the flat state. The changes are attributed to the increase in distance between atoms in ZnO [27, 28]. Fig. 3b

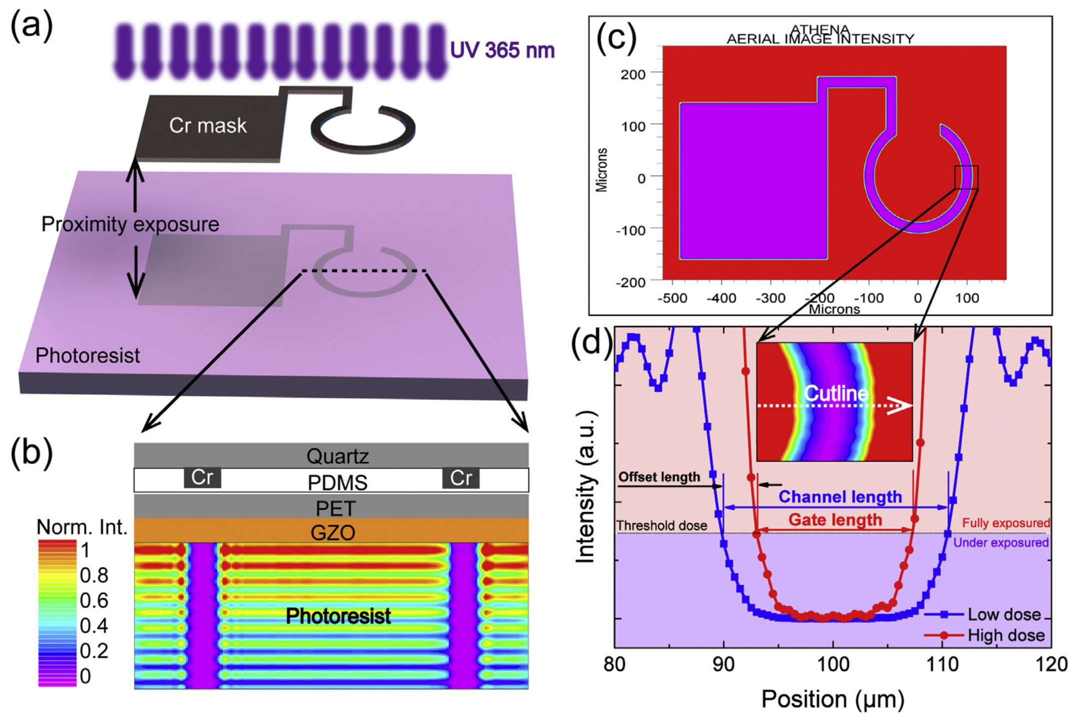

Fig. 2. (a) Schematic illustration of the proximity exposure method by separating the Cr mask and the photoresist to be exposed. (b) Normalized exposure intensity inside the photoresist. (c) Normalized exposure intensity contour of the Cr mask pattern. (d) Normalized exposure intensity profile along the cutline.

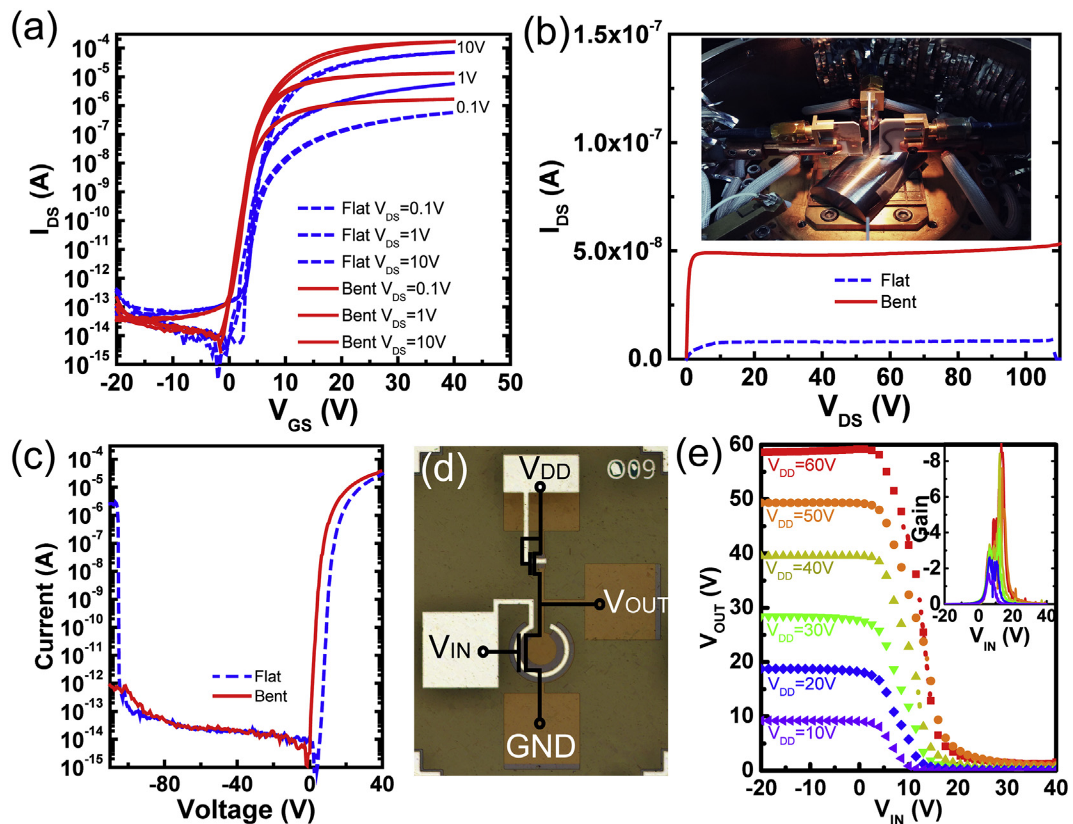

Fig. 3. (a) Transfer curves of the HVTFT in flat and bent states, respectively. (b) Output curves of the HVTFT in flat and bent states. (V_{GS} = 5 V), respectively. Inset is the picture of device under bending test (radius = 12 mm). (c) *I-V* characteristics of the HVTFD in flat and bent states, respectively. (d) Structure diagram of an HV inverter which is composed of an HVTFT drive and an on-chip HVTFD load. (e) Voltage-transfer curve of HV inverter when bent at a radius of 12 mm. Inset is its voltage gain.

shows the output curves of the HVTFT in flat and bent states (Inset photography) at $V_{GS} = 5$ V, respectively, with the maximum operation drain voltage above 110 V. Similarly, in the *I-V* test of the HVTFD, the bent state shows higher forward current and larger breakdown voltage than those in the flat state. Fig. 3d is the schematic diagram of HV inverter. The HVTFT acts as a closed switch with high-state V_{IN}, pulling V_{OUT} to ground, while it acts as an opened switch with low-state V_{IN}, pulling V_{OUT} to V_{DD}. Fig. 3e shows the voltage-transfer performance of the HV inverter on PET substrate, the inset demonstrating the voltage gain as high as 8.5.

3. Conclusion

In conclusion, we report flexible fully-transparent HV inverters, composed of an HVTFT drive and an on-chip HVTFD load. The HV devices were fabricated with a novel self-aligned technology, the fabrication process and working principle of which were introduced. The successful realization of high-performance flexible fully-transparent HVTFTs, HVTFDs and HV inverters will initiate interdisciplinary researches by drawing researcher from one field to the other.

Declarations of interest

None.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grants Nos. 11674405, 11675280, 11274366, 51272280, and 61306011). The authors acknowledge support from the Laboratory of Microfabrication in Institute of Physics, Chinese Academy of Sciences.

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