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2014 J. Phys. D: Appl. Phys. 47 255101

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Enhancement-mode ZnO/Mg_{0.5}Zn_{0.5}O HFET on Si

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Received 12 March 2014, revised 21 April 2014

Accepted for publication 25 April 2014

Published 20 May 2014

Abstract

We report a bottom-gate and enhancement-mode ZnO/Mg_{0.5}Zn_{0.5}O heterojunction field effect transistor (HFET) on Si. This new heterostructure which is grown by using molecular beam epitaxy (MBE) reduces interface defects and traps. By tailoring Mg composition (x) in the Mg _{x} Zn_{1- x} O barrier layer up to 50%, the Mg_{0.5}Zn_{0.5}O exhibits insulating properties and the resultant HFET works in an enhancement mode with a field effective mobility of $\mu_{FE} = 21 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, transconductance of $g_m = 44 \text{ mS mm}^{-1}$, on/off ratio of 1×10^5 and off current $\sim 1.33 \times 10^{-8} \text{ A mm}^{-1}$. The device shows good ambient stability.

Keywords: enhancement, ZnO/MgZnO, HFET, bottom-gate

(Some figures may appear in colour only in the online journal)

As a wide-band-gap semiconductor, ZnO has the merits of a low growth temperature, high electric breakdown field, good high temperature resistance, high electron saturation velocity and capabilities of wet etching processing. Furthermore, ZnO-based ternary alloys such as Mg _{x} Zn_{1- x} O extend the band gap, enabling the engineering of both the energy band and electrical properties. In particular, field effect transistors (FETs) using a ZnO/MgZnO heterojunction structure are expected to achieve the low-power-loss and high-speed switching performance. Many groups have also proved that the ZnO/MgZnO heterostructure has many excellent properties such as good radiation hardness [1], high bandwidth [2] and high mobility [3]. Up to date, all the reported ZnO heterojunction field effect transistor (HFETs) are built on the lattice-matched insulating substrates. For real applications, integration of ZnO HFETs with Si is highly expected mainly due to the availability of large diameter substrates, mature microelectronic technologies, better thermal conductivity of Si ($1.4 \text{ W cm}^{-1} \text{ K}^{-1}$) than ZnO ($0.6 \sim 1 \text{ W cm}^{-1} \text{ K}^{-1}$) [4] and possibility for simple vertical device structures and fabrication processes.

From the intensively studied GaN/AlGaIn HFETs it can be seen that the layer structure and gate insulator play key roles in the device's performance, particularly in the realization of the enhancement-mode (E-mode) HFET [5, 6]. The traditional Schottky gate HFETs usually suffer from a large gate leakage current while MOS-HFETs or MIS-HFETs need additional deposition of a thin gate dielectric material, such as Al₂O₃, SiO₂, SiN _{x} and HfO₂ [7–9]. Generally, the gate dielectric layers are not deposited in the same chamber without vacuum break, leading to the presence of interface defects and traps due to the interrupted interface and contaminated surface [10–12].

In this letter, we report a new ZnO/Mg _{x} Zn_{1- x} O HFET. In contrast to all previously reported results, this HFET is built on Si, which has a different lattice structure from ZnO. The device possesses the bottom-gate (B-gate) configuration as shown in figure 1(a). A ZnO/Mg _{x} Zn_{1- x} O heterostructure is grown by radio-frequency plasma assisted molecular beam epitaxy (rf-MBE) on a p-Si (111) with a resistivity of $0.1 \sim 1 \Omega \text{ cm}$, which serves as the common gate and as the substrate. The detailed layer structure is schematically depicted in figure 1(b). The Mg _{x} Zn_{1- x} O plays two roles in the device: as the barrier layer in the ZnO/MgZnO heterojunction and as the gate

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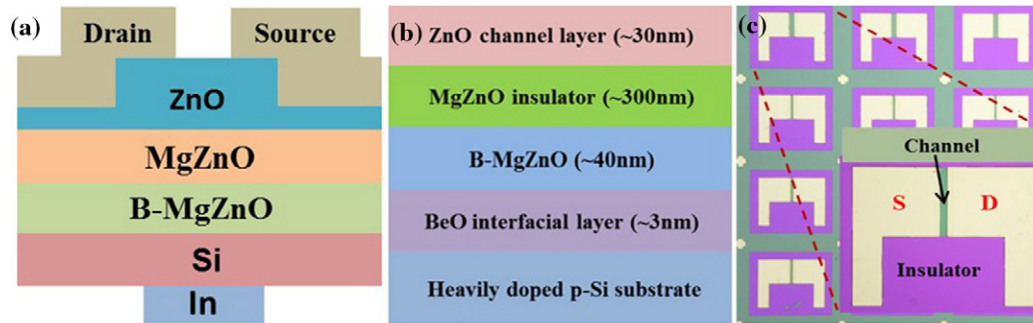


Figure 1. (a) Schematic diagram of a ZnO/MgZnO/Si HFET, (b) top view of ZnO HFET in optical microscope and (c) layer structure of MBE grown film.

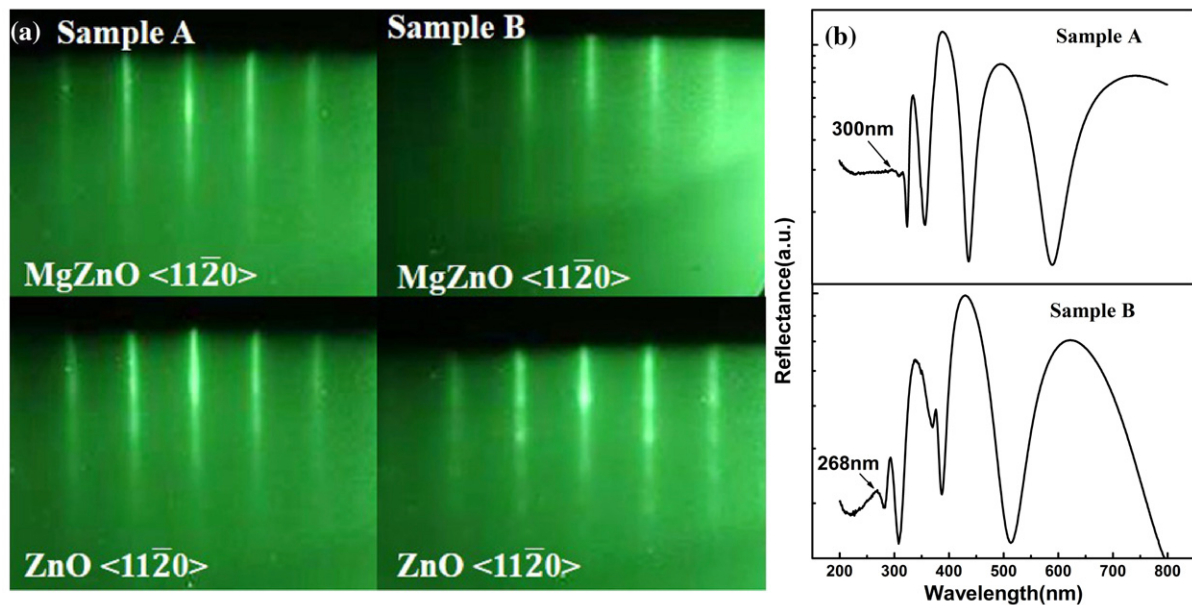


Figure 2. (a) RHEED patterns of the ZnO layer and MgZnO insulator as recorded in sample synthesis and (b) reflectance spectra of $\text{Mg}_x\text{Zn}_{1-x}\text{O}$ ($x = 0.4$ and 0.5) films.

dielectric oxide in the B-gate MOS-HFETs. In this case, it is desirable that the MgZnO layer exhibits high single crystalline quality and high Mg content, because the MgZnO with a higher Mg composition will own a larger band gap and better insulating properties compared to the lower-Mg-content MgZnO layer. It has been found that an interfacial layer with a 4-coordinated bonding configuration is essential to avoid the occurrence of phase separation in MgZnO, which heavily restricts the increase of Mg content and the band gap, as well as the delicate control of the electrical properties [13]. To get a MgZnO insulating layer with a high Mg content, a 3 nm wurtzite BeO interfacial layer was firstly formed on Si by oxidation of Be to protect the clean Si surface and provide a good template for wurtzite MgZnO epitaxy. A 40 nm MgZnO buffer (B-MgZnO) layer with low Mg content was deposited subsequently in order to relax the big lattice strain between the substrate and the following high-Mg-content MgZnO epilayer (300 nm) [14]. The ZnO channel layer (~ 30 nm) with an electron concentration of $2.04 \times 10^{17} \text{ cm}^{-3}$ was then grown on MgZnO. During the whole growth, the temperature of the Zn Knudsen cell was kept at 310°C , while the temperature

of Mg cell was set at 340°C for B-MgZnO. To investigate the influence of different Mg compositions in the $\text{Mg}_x\text{Zn}_{1-x}\text{O}$ epilayer on HFET performances, the temperature of the Mg cell was increased from 363 to 371°C for the MgZnO epilayer growth, corresponding to the samples labelled as A ($x = 0.4$) and B ($x = 0.5$), respectively.

It should be noted that BeO has a higher dielectric constant (~ 6.8) than SiO_2 (3.9), and its electron affinity (χ) and bulk band gap are 1.7 eV and 10.6 eV, respectively [15]. The band alignment between BeO and Si is calculated as 3.47 eV for CBO (conduction band offset) and 7.13 eV for VBO (valence band offset). However, the 3 nm BeO layer is so thin that it cannot serve as an efficient dielectric barrier layer to block carriers from both the Si and B-MgZnO sides [16]. So it will be ignored in our following discussion regarding the carrier transportation process in this multilayer structure.

The HFETs were fabricated by the standard photolithograph and lift off technique. Ti (20 nm)/Au (50 nm) was deposited to form drain and source electrodes on the ZnO channel layer by thermal evaporation, and indium as the back contact to p-Si [17]. The active layer was fixed at a width and length of

150 μm and 10 μm , respectively (the top view of the devices is shown in figure 1(c)). All the electrical tests were conducted in the dark using an Agilent B1500A semiconductor parameter analyser.

Shown in figure 2(a) are the reflected high-energy electron diffraction (RHEED) patterns of MgZnO and ZnO films in samples A and B, respectively. The six-fold symmetrical patterns are seen in both of the samples, indicating that ZnO/Mg_xZn_{1-x}O has the single-phase wurtzite structure with a high crystal quality. The streaky lines imply the sharp and smooth interface morphology. More importantly, the spacings between the reciprocal lattice rods (the streaky lines) essentially remain the same for ZnO and MgZnO in both the electron-beam azimuths, suggesting nearly unchanged lattice constants for ZnO and MgZnO. So the growth of ZnO on Mg_xZn_{1-x}O follows a quasi-homo epitaxy mode, lattice strains induced in the ZnO channel layer is minimal, the crystalline quality of ZnO thin film can be ensured and the electron concentration and mobility of ZnO epilayers can be elaboratively modulated during the growth. The Mg compositions of the two Mg_xZn_{1-x}O samples have been determined by Rutherford backscattering spectrometry (RBS) measurements as 40% and 50% (not shown here), respectively. The optical band gap of these two samples is determined as 4.13 eV (300 nm) and 4.63 eV (268 nm), respectively, from the peak positions indicated by the arrows in room-temperature reflectance spectra (figure 2(b)). The band gap values match up well with the RBS results.

Figures 3(a) and (b) show the output characteristics of the B-gate ZnO HFETs with Mg_{0.4}Zn_{0.6}O and Mg_{0.5}Zn_{0.5}O as gate insulators, respectively. The devices show saturation current with a high drain bias in both of the source-to-drain current curves. When $V_{\text{ds}} < 1$ V, there is a negative current. In the sample with Mg_{0.5}Zn_{0.5}O as the gate insulator, the negative current was well suppressed and the saturation current was much lower than the device with 40% Mg content, indicating the better insulating properties of the Mg_{0.5}Zn_{0.5}O dielectric layer. This can be further confirmed by $I_{\text{g}} - V_{\text{g}}$ characteristics, as shown in figure 3(c). The vertical leakage current in sample B is one order of magnitude lower than sample A, at a level of 10^{-7} A at $V_{\text{g}} = 0.8$ V. We think that large leakage current has a bad influence on the device's performance, such as a high off current.

Figures 4(a) and (b) display the $I_{\text{DS}} - V_{\text{G}}$ and $g_{\text{m}} - V_{\text{G}}$ curves at $V_{\text{DS}} = 10$ V with two different Mg concentrations. For ZnO/Mg_{0.4}Zn_{0.6}O HFET a saturation mobility μ_{sat} of $1.83 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was obtained at $V_{\text{ds}} = 10$ V, a field effect mobility of $\mu_{\text{FE}} = 1.52 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ based on the linear $I - V$ curve at $V_{\text{ds}} = 0.5$ V and a peak g_{m} of 19.8 mS mm^{-1} . Here μ_{sat} is calculated from $I_{\text{DS}} = \mu_{\text{sat}} C_{\text{i}} (V_{\text{G}} - V_{\text{T}})^2 W (2L)^{-1}$ and $\mu_{\text{FE}} = g_{\text{m}} L (C_{\text{i}} W V_{\text{ds}})^{-1}$, where I_{DS} is the source-drain current, C_{i} is the capacitance per unit area of the gate insulator layer, V_{G} is the gate voltage, V_{T} is the threshold voltage and g_{m} is the transconductance value. This device shows a depletion (D-mode) type of characteristic and the on/off ratio of I_{DS} is only ~ 300 , and the turn-on voltage (V_{on}) is about -1 V. However, when we increased the Mg composition up to 50%, firstly, the leakage current had minimized, then the B-gate

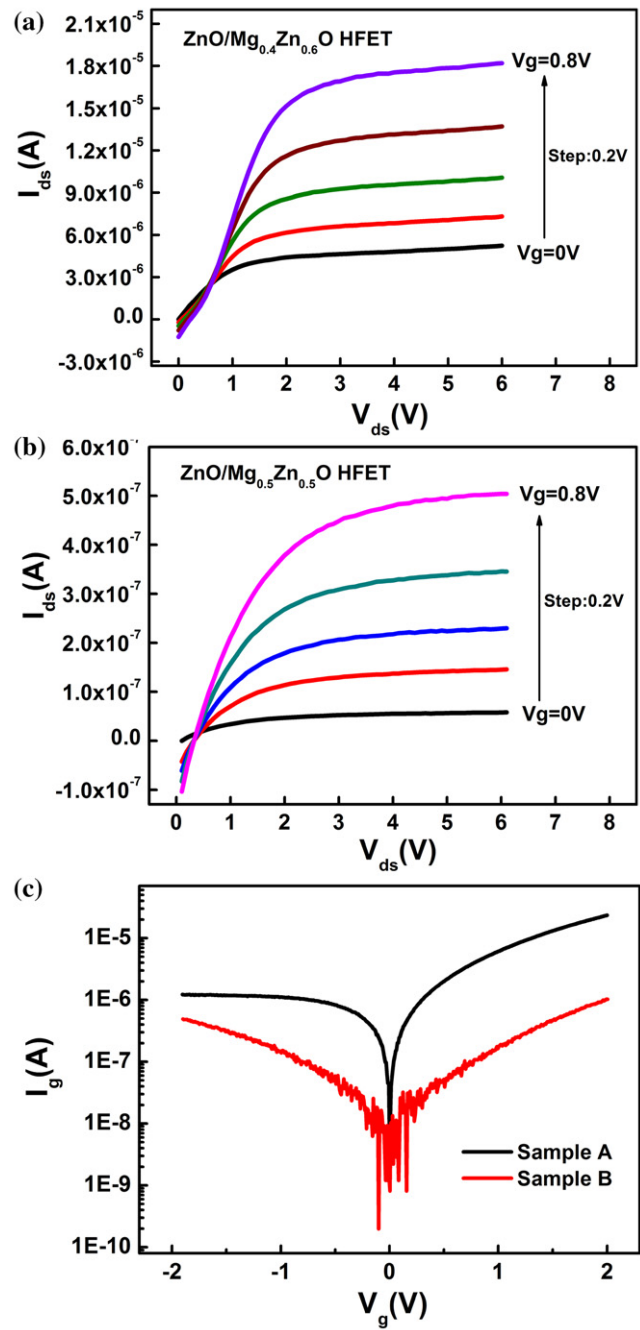


Figure 3. (a) $I_{\text{ds}} - V_{\text{ds}}$ characteristics of ZnO/Mg_{0.4}Zn_{0.6}O/Si HFET, (b) $I_{\text{ds}} - V_{\text{ds}}$ characteristics of ZnO/Mg_{0.5}Zn_{0.5}O/Si HFET and (c) $I_{\text{g}} - V_{\text{g}}$ characteristics of two ZnO/Mg_xZn_{1-x}O ($x = 0.4$ and 0.5) HFETs.

HFET showed a much higher mobility ($\mu_{\text{sat}} = 21 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $V_{\text{ds}} = 10$ V and $\mu_{\text{FE}} = 19.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $V_{\text{ds}} = 0.5$ V) and higher transconductance ($g_{\text{m}} = 44 \text{ mS mm}^{-1}$). The on/off ratio reaches 1×10^5 , and the off current is reduced to $\sim 1.33 \times 10^{-8} \text{ A mm}^{-1}$. When the gate voltage is equal to 0 V, the drain current is close to the lowest level. The 'normally off' behaviour indicates that the device works under a real enhancement mode. V_{on} is widely preferable to V_{T} as a practical device performance metric, as it directly characterizes the gate voltage required to fully 'turn off' the transistor in

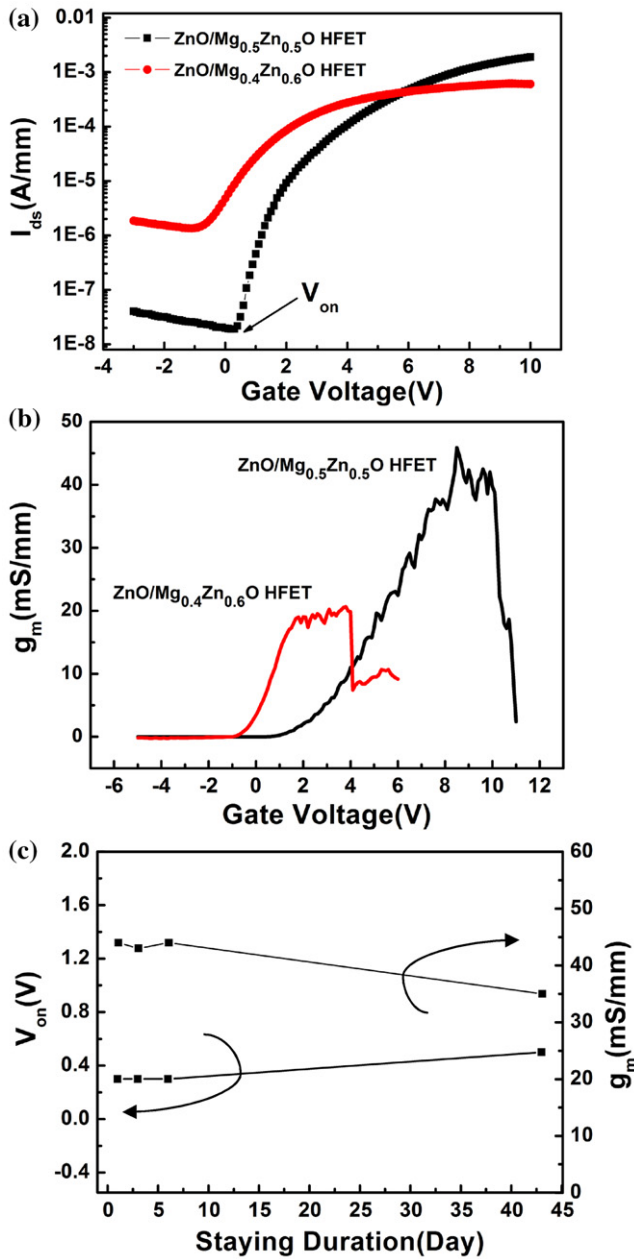


Figure 4. (a) Transfer characteristics of ZnO/Mg_xZn_{1-x}O ($x = 0.4$ and 0.5) HFETs, (b) $g_m - V_{gs}$ characteristics of ZnO/Mg_xZn_{1-x}O ($x = 0.4$ and 0.5) HFETs, and (c) variation of V_{on} and g_m of ZnO/Mg_{0.5}Zn_{0.5}O/Si HFET in a time period of 42 days at atmospheric pressure.

a switching application (as shown in figure 4(a)) [18]. To confirm the ambient stability of the B-gate ZnO/MgZnO/Si HFETs, the time-dependent V_{on} and g_m values were measured in a time period of 42 days at atmospheric pressure. Figure 4(c) shows that V_{on} and g_m stay well in ~ 0.4 V and ~ 40 mS mm⁻¹ levels during the test.

To interpret the principle of our B-gate HFETs, the energy band diagram of ZnO/Mg_xZn_{1-x}O/Si is drawn according to the Anderson–Shockley model as shown in figure 5. The electron affinity (χ) and band gap for ZnO and Si are taken as 4.35 and 4.05 eV, 3.37 and 1.12 eV, respectively [19]. The electron concentration in Mg_xZn_{1-x}O will decrease when Mg

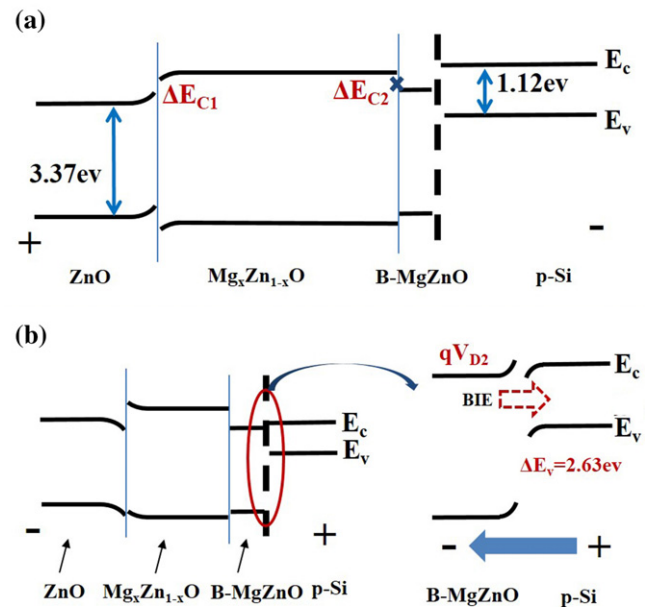


Figure 5. The energy band diagram of the ZnO/Mg_xZn_{1-x}O/Si structure: (a) under negative gate voltage and (b) under positive gate voltage.

content increase, i.e., the higher Mg content, the lower electron concentration.

When the negative voltage is applied on the gate electrode (Si substrate side) (figure 5(a)), the electrons in the channel layer have been depleted and no channel current is flowing. In the case of the Mg_{0.4}Zn_{0.6}O dielectric layer, there are still remarkable residual carriers resulting in a high off-current ($\sim 10^{-6}$ A mm⁻¹) and negative turn-on voltage ($V_{on} < 0$). While Mg content increases from 40% to 50%, the band gap of MgZnO increases from 4.13 to 4.63 eV. It has been reported that the incorporation of Mg into H_fO₂ and ZnO can effectively reduce oxygen vacancies. Consequently, a higher Mg content indicates the existence of more Mg-O bonds and a remarkable decrease of oxygen vacancy density in MgZnO [20, 21]. As a result, the background electron concentration in Mg_{0.5}Zn_{0.5}O can be lower than 10^{14} cm⁻³, and these fewer residual electrons result in a lower off current ($\sim 1.33 \times 10^{-8}$ A mm⁻¹) and the enhancement mode operation ($V_{on} = 0$).

Under equilibrium, the carrier's diffusion introduces an energy barrier known as a built-in electric field (BIE) between n-type B-MgZnO and p-Si, which is calculated as $qV_{D2} = 0.6$ eV, blocking most of the electrons in B-MgZnO (the electron concentration is 2.14×10^{16} cm⁻³). However, the device shows different behaviours under the forward gate bias (figure 5(b)). On the one hand, some electrons can jump into the MgZnO dielectric layer from the ZnO channel layer because the ΔE_c between this type-I heterojunction is just 0.68 eV for the case of the Mg content of 40%. On the other hand, the BIE between B-MgZnO and Si will be lowered by the applied external electric field, so the electrons can be injected into the Si side (the gate electrode) and form a leakage current. Consequently, a negative current in output characteristics was observed. Suppression of this leakage current can be achieved

by increasing the Mg content of the B-Mg_xZn_{1-x}O layer later, as shown in figures 3(b) and (c).

The Mg_xZn_{1-x}O with high Mg content shows good insulating properties including a high dielectric permittivity (~10) and breaking voltage [22, 23]. Mg atoms can effectively reduce the density of oxygen vacancies which act as the main native defects in ZnO [20]. In Mg_{0.5}Zn_{0.5}O alloy, the carrier concentration is lower than 10¹⁴ cm⁻³, and the electron mobility is <0.01 cm² V⁻¹ s⁻¹ [16]. When Mg content is higher than 40%, the ΔE_v is larger than 2.6 eV, which is enough to block the holes from the Si substrate and thus the leakage current can be significantly reduced [24]. The unique advantage is that the ZnO active layer and Mg_xZn_{1-x}O dielectric layer are deposited in the MBE chamber successively; thus there is no need for a Schottky contact or an additional gate dielectric layer in this new device structure, resulting in the decrease of interface defects and traps, as well as improvement of the device's performance and simplification of fabrication process.

As we all know, the polarization effects on the generation of channel carriers in HFETs, both for AlGaIn/GaN and MgZnO/ZnO, relies upon the polarity selections. The polarity of ZnO and MgZnO can be delicately controlled on a sapphire substrate by changing the MgO buffer layer thickness [25] or nitridation temperature [26, 27]. The polarization-induced two-dimensional electron gas (2DEG) and quantum Hall effect have been excitingly reported in an O-polar ZnO/MgZnO heterojunction grown on the ScAlMgO₄ (0001) substrate [28]. The ZnO/MgZnO heterojunction on Si, however, remains unexplored due to the formidable challenge of single crystal film growth and polarity control. Fortunately, we developed a unique BeO-buffered interface engineering technique, and with this a ZnO/MgZnO heterojunction with a smooth surface and interface can be achieved. However, determining the polarity and 2DEG formation of Si still remains a challenge. Consequently we did not claim the existence of 2DEG in our device. On the other hand, 2DEG in AlGaIn/GaN HFETs has not been found effective for the realization of enhancement-mode transistors, although it has been widely investigated in high electron mobility transistor (HEMT) fabrication. Therefore another issue yet to be addressed is if there is 2DEG in our HFET, and if so what role it plays in the achievement of the enhancement working mode.

In summary, a new enhancement-mode ZnO/Mg_{0.5}Zn_{0.5}O HFET with a bottom-gate configuration has been fabricated on an Si substrate. The device shows a field effective mobility of μ_{FE} = 21 cm² V⁻¹ s⁻¹, a transconductance of g_m = 44 mS mm⁻¹, an on/off ratio of 1 × 10⁵, an off current of ~1.33 × 10⁻⁸ A mm⁻¹ and good ambient stability. The improved performance is ascribed to the decreased interface defects in the new B-gate device structure and the good insulating properties of Mg_{0.5}Zn_{0.5}O.

This work was supported by the Ministry of Science and Technology of China (Grant nos 2011CB302002, 2011CB302006), the National Science Foundation of China

(Grant nos 11174348, 51272280, 11274366, 61204067, 61306011), and the Chinese Academy of Sciences.

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